WHAT IS CLAIMED IS:

1. A test pattern for measuring a contact resistance, comprising:

a test wafer in which a plurality of device isolation films are formed to define a plurality of active regions;

a plurality of interconnection diffusion layer formed in a word line region crossing the plurality of the device isolation films and the plurality of the active regions;

a plurality of source diffusion layers formed in a first line contact region located at one side of said word line region;

a plurality of source diffusion layers formed in a second line contact region located at the other side of said word line region; and

a plurality of line contact pattern formed in said first and second line contact regions,

wherein said line contact pattern formed in said first line contact region and said line contact pattern formed in said second line contact region are alternately positioned and wherein current for measuring a resistance flows along said first line contact region and said second line contact region between said word line in a three-dimensional manner.

2. The test pattern for measuring a contact resistance as claimed in claim 1, wherein said word line region, said first line contact region and said second line contact region are juxta-positioned.

3. The test pattern for measuring a contact resistance as claimed in claim 1, wherein said source diffusion layer in said first line contact region and said source diffusion layer in said second line contact region are electrically connected by an interconnection diffusion layer in said word line region.

4. The test pattern for measuring a contact resistance as claimed in claim 1, wherein one of the plurality of the line contact patterns in said first line contact region electrically connects two of the plurality of the source diffusion layers in said first line contact region and is isolated/positioned from another line contact pattern.

5. The test pattern for measuring a contact resistance as claimed in claim 1, wherein one of the plurality of the line contact patterns in said second line contact region electrically connects two of the plurality of the source diffusion layers in said second line contact region and is isolated/positioned from another line contact pattern.

6. A method of manufacturing a test pattern for measuring a contact resistance

forming a plurality of device isolation films in a test wager to define a plurality of active regions;

performing an impurity ion implantation process to simultaneously form a source diffusion layer in a plurality of active regions of a first line contact region, an interconnection diffusion layer in a plurality of active

regions of a word line and a source diffusion layer in a plurality of active regions of a second line contact region;

forming a word line surrounded by an insulating film spacer in said word line region;

forming an insulating layer the surface of which is flattened on the entire structure including said word line;

forming a self-aligned contact mask on said insulating layer; and

forming a plurality of line contact patterns in said first and second line contact regions through a self-aligned contact process using said self-aligned contact mask,

wherein said line contact pattern formed in said first line contact region and said line contact pattern formed in said second line contact region are alternately positioned and current for measuring a resistance flows along said first line contact region and said second line contact region between said word line in a three-dimensional manner.

7. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 6, wherein said word line region, said first line contact region and said second line contact region are juxta-positioned crossing the plurality of the device isolation films and the plurality of the active regions.

8. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 6, wherein said source diffusion layer in said

first line contact region and said source diffusion layer in said second line contact region are electrically connected by an interconnection diffusion layer in said word line region.

9. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 6, wherein one of the plurality of the line contact patterns in said first line contact region electrically connects two of the plurality of the source diffusion layers in said first line contact region and is isolated/positioned from another line contact pattern.

10. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 6, wherein one of the plurality of the line contact patterns in said second line contact region electrically connects two of the plurality of the source diffusion layers in said second line contact region and is isolated/positioned from another line contact pattern.

11. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 6, wherein said self-aligned contact mask is formed to cover an upper portion of said word line, an upper portion of a portion of said device isolation film between said first source diffusion layer and said second source diffusion layer in said first line contact region, and an upper portion of a portion of said device isolation film between said second source diffusion layer and said third source diffusion layer in said second line contact region.

12. A method of manufacturing a test pattern for measuring a contact resistance

forming a plurality of device isolation films in a test wafer to define a plurality of active regions;

performing a threshold voltage ion implantation process to form a threshold voltage ion implantation region in the plurality of the active regions in a word line region;

forming a word line in said word line region;

performing an impurity ion implantation process to form a source diffusion layer in each of the plurality of the active regions of a first line contact region and a source diffusion layer in each of the plurality of the active regions of a second line contact region;

forming an insulating film spacer surrounding said word line;

forming an insulating layer the surface of which is flattened on the entire structure including said word line;

forming a self-aligned contact mask on said insulating layer; and

forming a plurality of line contact patterns in said first and second line contact regions through a self-aligned contact process using the self-aligned contact mask,

wherein said line contact pattern formed in said first line contact region and said line contact pattern formed in said second line contact region are alternately positioned and current for measuring a resistance flows along said first line contact region and said second line contact region between said word

line in a three-dimensional manner.

13. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 12, wherein said word line region, said first line contact region and said second line contact region are juxta-positioned crossing the plurality of the device isolation films and the plurality of the active regions.

14. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 12, wherein the source diffusion layer in the first line contact region and the source diffusion layer in the second line contact region are electrically connected by a channel formed in a threshold voltage ion implantation region by applying a voltage to the word line in said word line region.

15. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 12, wherein one of the plurality of the line contact patterns in said first line contact region electrically connects two of the plurality of the source diffusion layers in said first line contact region and is isolated/positioned from another line contact pattern.

16. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 12, wherein one of the plurality of the line contact patterns in said second line contact region electrically connects two of

the plurality of the source diffusion layers in said second line contact region and is isolated/positioned from another line contact pattern.

17. The method of manufacturing a test pattern for measuring a contact resistance as claimed in claim 12, wherein said self-aligned contact mask is formed to cover an upper portion of said word line, an upper portion of a portion of said device isolation film between said first source diffusion layer and said second source diffusion layer in said first line contact region, and an upper portion of a portion of said device isolation film between said second source diffusion layer and said third source diffusion layer in said second line contact region.